CLOCK SKEW TOLERANT CLOCKING SCHEME

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ABSTRACT OF THE DISCLOSURE

A clock skew tolerant clocking scheme addresses both the max-time and min-time problems by using dual transparent pulsed latches operated by complementary phases of the clock signal. According to the present invention, the first pulsed latch is triggered by a first pulse derived by the leading edge of a clock signal pulse and the second pulsed latch is triggered by a second pulse derived from the trailing edge of the clock signal. By employing transparent pulse latches, the clock skew tolerant clocking scheme of the invention provides max-time clock skew tolerance. In addition, unlike prior art solutions, according to the invention, the transparency periods of the dual complementary pulsed latches do not overlap so there is never a transparency period between two successive stages and, therefore, there is no opportunity to introduce the min-time, or racing condition, problem.